Sierra Components, Inc.

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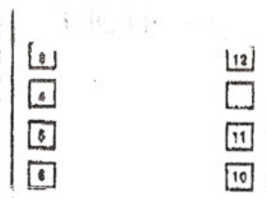
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Pad	Functi			
1	Collector Q1	8	Collector Q3	
2	Base Q1	9	Base Q4	
3	Emitters Q1/Q2	10	Emitter Q4	
4	Base Q2	11	Collector Q4	
5	Collector Q2	12	Base Q5	
6	Base Q3	13	Emitter Q5	
7	Emitter Q3	14	Collector Q5	

: Chip back must be connected to V-.

For orientation bond pad 1 metal is circular.

NC = No Conn

·e information on this layout is believed to be correct. ·ability for error or omission can be accepted. The supply ·ce to this layout can only be guaranteed if it forms part o specification, or the chip identification, if below, is reques Chip back potential is the level at which bulk silicor maintained by on-chip connection. It is not to be interprete.. a mounting recommendation unless specifically stated above. If no potential is given the ch·p should be isolated. Nominal metal thicknesses ınufacturer's information.

Topside Metal: Al
Backside: Si
Backside Potential: V-
Mask Ref:
Bond Pads: .004" min

APPROVED BY:CB	**DIE SIZE: .053" x .052"**	**DATE: 1/26/01**
MFG: HARRIS	**THICKNESS: .019"**	**P/N: HFA3046**